IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application of

Applicant	: David L. Chapek
Serial No.	: 09/605,293
Filed	: June 28, 2000
Title	: SEMICONDUCTOR DEVICES INCLUDING A LAYER OF POLYCRYSTALLINE SILICON HAVING A SMOOTH MORPHOLOGY
Docket No.	: MIO 0037 VA (96-0831.01)
Examiner	: N.D. Richards
Art Unit	: 2815

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 28, 2005.

Susan M. Luna
Agent Reg. No. 38,769

Sir:

APPEAL BRIEF

This is an appeal from the Office Action mailed December 10, 2004, finally rejecting claims 9-12 and 14 in the application. A Notice of Appeal was timely filed on March 7, 2005, with the accompanying fee. Our check in the amount of $500 accompanies this Brief in accordance with 37 CFR §41.20(b)(2).

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office at Reel 9159, Frame 0921.

Related Appeals and Interferences

Applicant knows of no currently pending related appeals or interferences that would have an effect on the outcome of this appeal.

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Status of Claims

Claims 9-12 and 14 are pending in this application and are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

No amendments to the claims were filed after final rejection. All previous amendments have been entered.

Summary of Claimed Subject Matter

One embodiment of the present invention is directed to a semiconductor device or substrate which incorporates a layer of silicon dioxide which has been pretreated to provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon. The pretreatment method includes implanting hydrogen ions into a layer of silicon dioxide by plasma source ion implantation and forming a layer of polycrystalline silicon on the layer of silicon dioxide such that the polycrystalline silicon layer is free of contaminants and has a smooth morphology.

In one embodiment of the invention illustrated in Fig. 1 and described at pages 7-10 of the specification, the layer 14 of silicon dioxide 16 comprises a layer in a semiconductor substrate 12. After the layer is doped by plasma source ion implantation, a layer 18 of polycrystalline silicon 20 is formed on the layer 14 of silicon dioxide.

In another embodiment illustrated in Fig. 2 and described at pages 10-11, the layer of silicon dioxide comprises a layer in a semiconductor substrate 52 which is part of a field effect transistor 50 comprising a gate oxide 54 and a source 56 and drain 58 formed on the semiconductor substrate. A layer of polysilicon 66 is formed on the gate oxide 54 to form a gate electrode 70. The surface of the substrate 52 is pretreated as described above so that the subsequently formed layer 64 of polysilicon 66 has a smooth morphology.

In another embodiment shown in Fig. 3 and described at page 12, the silicon dioxide layer may be formed on a semiconductor substrate which is part of a memory array 100 including a plurality of memory cells 102 which comprise at least one field effect transistor 50, a gate oxide for each of the field effect transistors, a source and drain for each of the field effect transistors, and a gate electrode for each of the field effect transistors.

In another embodiment illustrated in Fig. 4 and described at page 12, the layer of silicon dioxide is formed on a semiconductor substrate 52 which is incorporated in a semiconductor wafer W which comprises a repeating series of gate oxides, a repeating series of sources and drains, and a repeating series of gate electrodes.

In another embodiment illustrated in Fig. 5 and described at pages 13-14, a layer of silicon dioxide, glass or quartz comprising a semiconductor substrate 202 is doped with hydrogen ions as described above and then deposited with a layer of polycrystalline silicon 206. The semiconductor substrate is incorporated into a thin film transistor 200 which includes a gate oxide, a source and drain region formed in the polycrystalline silicon layer, and a gate electrode.

Grounds of Rejection to be Reviewed on Appeal

The grounds of rejection for review on appeal are:

1) Claims 9-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art" with Henley et al. (U.S. 6,083,324)

2) Claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "Applicant's admitted prior art" and Henley et al.

Grouping of Claims

The Examiner has made two grounds of rejection, rejecting claims 9-12 under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art" with Henley et al. (U.S. 6,083,324); and rejecting claim 14 under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. 5,576,229) in view of "Applicant's admitted prior art" and Henley et al. The application contains five rejected independent claims, namely, claims 9, 10, 11, 12, and 14. Applicant submits that the claims do not stand or fall together. The patentability of claim 9 as representative of claims 9-12 will be separately argued. The patentability of claim 14 will also be separately argued.

Argument

Rejection under 35 U.S.C. 103(a) over Burns et al. (Principles of Electronic Circuits, pp. 380-381) in view of "Applicant's admitted prior art" and Henley et al

Claim 9

Claim 9 recites, inter alia, a semiconductor device precursor comprising a silicon dioxide layer on a semiconductor substrate. The surface of the silicon dioxide layer has been doped with hydrogen ions deposited by a plasma ion implantation process and is free of sputtered metal contaminants. A layer of polycrystalline silicon is formed on the layer of silicon dioxide and has a smooth morphology.

Burns et al. teach a field effect transistor including a source and drain, a layer of silicon dioxide, and a gate electrode formed of aluminum. Henley et al. teach a method of providing a gettering layer in a silicon-on-insulator wafer using a plasma immersion ion implantation technique to implant ions, gas, or carbon as precipitate-forming particles beneath the surface of the silicon wafer, but above the surface of the insulating oxide layer. By "Applicant's admitted prior art," the Examiner is referring to the discussion of the prior art Kaufman ion source implantation technique discussed at page 1, lines 12-22 of applicant's specification. That technique results in metal contamination on the surface of the target object.

In the Advisory Action mailed February 7, 2005, the Examiner admitted that Henley et al. do not expressly teach that their implantation technique could be applied to the surface of a silicon dioxide layer. However, he maintained that it would have been obvious to one skilled in the art to have done so, reasoning that one would recognize that if a process can implant below the surface, "one would only need to reduce the implantation energy to implant into the surface." The Examiner further reasoned that one would reasonably expect the silicon dioxide layer to be free of metal contaminants as claimed because the "admitted prior art" teaches that the source of metal contamination is a result of the implantation apparatus and "Henley et al. expressly teach that their method sometimes produces less contamination."

Applicant disagrees with the Examiner's reasoning as well as his ultimate conclusion. The Examiner has failed to carry his burden of establishing a prima facie case of obviousness. As applicant previously pointed out, Henley's teaching that "in some instances" their implantation technique produces less metal contamination than other ion implantation techniques does not provide motivation for one to substitute Henley's technique of implanting ions <u>beneath the surface</u> of a silicon wafer as a <u>surface</u> treatment in the absence of some suggestion from the prior art to do so. The Examiner's assumption that Henley's technique would be successful as a surface treatment has no factual basis and clearly impermissibly relies on <u>applicant's</u> invention as the source of such assumption.

While the Examiner opines that one would need only to reduce implantation energy to implant on the surface as opposed to below the surface, he has pointed to no reference which suggests such a modification. In order to establish a *prima facie* case of obviousness, there must be some objective teaching in the prior art that would lead one to combine the relevant teachings of the references. MPEP §2142.

Nor would one skilled in the art be motivated to combine the teachings of the references as Henley et al. do not teach or suggest that their implantation technique may be used for the purpose of providing a smooth morphology for a subsequently deposited layer of polycrystalline silicon. As taught by applicant at page 10, lines 2-5, the implantation of hydrogen ions in the silicon dioxide substrate is believed to increase the number of nucleation sites for the subsequent polycrystalline silicon deposition. Henley et al. do not address the same problem as the present

invention, and provide no expectation of a successful solution of that problem. Henley implants "gas-forming particles or ions" beneath a silicon wafer surface for the purpose of generating microbubbles or precipitates. In combining the teachings of the references, the Examiner cannot ignore the fact that Henley et al. do not teach a surface treatment, do not address the same problem, and provide no expectation of a successful solution of that problem. Nor do Henley et al. teach or suggest the specific use of hydrogen plasma ions; rather, Henley et al. teach a variety of ions, gases and carbon for use in implantation, with no suggestion that hydrogen ions should be chosen.

The reference teachings do not suggest any desirability or motivation to combine, nor do they provide any reasonable expectation of success. Claim 9 is clearly patentable because no prima facie case of obviousness has been established.

Claim 10

Claim 10 recites a field effect transistor which includes a silicon dioxide layer having hydrogen ions implanted on its surface, a layer of polycrystalline silicon formed on the layer of silicon dioxide having a smooth morphology, and a gate oxide formed on the semiconductor substrate. In the final rejection, the Examiner maintained that in view of the combined references, it would have been obvious to form the gate oxide of Burns et al. from a layer of silicon dioxide having hydrogen ions implanted therein such that the layer of polycrystalline silicon formed on the silicon dioxide would have a smooth morphology. As discussed extensively above, Henley does not address the problem, there is no suggestion in Henley et al. to implant hydrogen ions on the surface of a layer of silicon dioxide in a semiconductor substrate, nor is there any suggestion that such implantation would provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon. Nor is there any teaching or suggestion in Henley et al. of doing so on a silicon dioxide layer in a field effect transistor.

Claim 10 is believed to be patentable for these reasons.

Claim 11

Claim 11 recites a memory array including a semiconductor substrate with a silicon dioxide layer on the substrate having hydrogen ions implanted on its surface, and a layer of polycrystalline silicon formed on the layer of silicon dioxide having a smooth morphology. The Examiner maintains that Burns et al. disclose a read-only memory structure including a plurality of memory cells, asserting that it would have been obvious to form the gate oxide for each field effect transistor using a silicon dioxide layer having hydrogen ions implanted therein in view of "Applicant's admitted prior art" and Henley et al. Again, there is no teaching or suggestion in any of the references which would motivate one skilled in the art to combine their teachings to make the claimed memory array, nor do the cited references provide any expectation of success. Claim 11 is believed to be patentable for the same reasons discussed above.

Claim 12

Claim 12 recites a semiconductor wafer including a semiconductor substrate, with a silicon dioxide layer on the substrate having hydrogen ions implanted on its surface, and a layer of polycrystalline silicon formed on the layer of silicon dioxide having a smooth morphology. The Examiner maintains that one of ordinary skill in the art would have formed the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die as recited in claim 12. Again, the Examiner has failed to cite any reference, alone or in combination, which teaches or suggests such a semiconductor wafer in which the layer of silicon dioxide formed on the semiconductor substrate has been implanted with hydrogen ions on its surface as claimed. Claim 12 is clearly patentable over the cited references.

Rejection under 35 U.S.C. 103(a) over Murata et al. in view of Applicant's admitted prior art with Henley et al.

Claim 14

Claim 14 recites a thin film transistor comprising a semiconductor substrate formed from silicon dioxide, quartz, or glass which has been implanted on its surface with hydrogen ions by

plasma source ion implantation such that the substrate is free of metal contaminants, and a layer of polycrystalline formed on the substrate having a smooth morphology. Murata et al. teach a method of forming a thin film transistor on a glass substrate where hydrogen ions and metal ions are simultaneously implanted through a capping film and polysilicon film using a plasma source. The Examiner previously admitted at page 6 of the final rejection that Murata et al. do not teach a substrate which is free of metal contaminants as claimed, but reasons that it would have been obvious to implant hydrogen ions into the glass substrate of Murata et al. based on the teachings of "applicant's admitted prior art" and Henley et al. to achieve a substrate which is free of metal contaminants and in which a subsequently deposited polycrystalline silicon layer would have a smooth morphology.

Murata et al. do not address the same problem as the present invention, nor do they provide a solution to that problem. Rather, Murata et al. teach the implantation of hydrogen ions and metal ions into a semiconductor film for the purpose of obtaining a film having low resistivity. See col. 3, lines 27-37. Nor is there any suggestion in Henley et al. to implant hydrogen ions on the surface of a layer of silicon dioxide in a semiconductor substrate, nor any suggestion that such implantation would be successful and/or provide a smooth morphology for a subsequently deposited layer of polycrystalline silicon. Nothing in the prior art references provides motivation for preparing the glass surface of the substrate of Murata et al. such that it is free of metal contaminants and such that the subsequent deposition of a polycrystalline silicon layer has a smooth morphology as claimed. The combined teachings of "applicant's admitted prior art" and Henley et al. provide no motivation for one skilled in the art to use Henley's implantation technique in Murata.

Claim 14 is clearly patentable over the cited combination of references.

Conclusion

The Examiner has failed to establish a prima facie case, by evidence or reasoning, that any of the rejected claims would have been obvious with respect to the proposed combination of references. No motivation or suggestion exists to combine the teachings of the cited references. as none of the references teaches or suggests providing hydrogen ions implanted on the surface of a silicon dioxide substrate for the purpose of providing a subsequent layer of polycrystalline silicon which has a smooth morphology as claimed.

The Board is requested to reverse the rejections of claims 9-12 and 14 in their entirety.

Respectfully submitted,

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CLAIMS APPENDIX

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, the surface of said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process, wherein said layer of silicon dioxide is free of sputtered metal contaminants; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.

10. A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, the surface of said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a gate oxide formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain formed in said semiconductor substrate with a gate electrode formed on said semiconductor substrate from said layer of polycrystalline silicon to form a field effect transistor.

11. A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, wherein hydrogen ions are implanted into at least a portion of the surface of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor;

a gate oxide for each of said field effect transistors formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a source and a drain for each of said field effect transistors formed in said semiconductor substrate; and

a gate electrode for each of said field effect transistors formed on said semiconductor substrate from said layer of polycrystalline silicon.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die hydrogen ions are implanted into at least a portion of the surface of said layer of silicon dioxide by plasma source ion implantation, wherein said layer of silicon dioxide is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a repeating series of gate oxides formed on said semiconductor substrate from said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a repeating series of sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of sources and drains being formed on said semiconductor substrate; and

a repeating series of gate electrodes for at least one field effect transistor formed on each of said plurality of die, said series of gate electrodes being formed on said semiconductor substrate from said layer of polycrystalline silicon.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, the surface of said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation, wherein said semiconductor substrate is free of sputtered metal contaminants;

a layer of polycrystalline silicon formed on at least a portion of said semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of an insulating material formed on at least a portion of said layer of polycrystalline silicon;

a gate oxide formed from said layer of insulating material;

a source region and a drain region formed in said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

PTO/SB/17 (12-04)
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/605,293
Filing Date	June 28, 2000
First Named Inventor	David L. Chapek
Examiner Name	N.D. Richards
Art Unit	2815
Attorney Docket No.	MIO 0037 VA/40509.118

METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): ____

☐ Deposit Account Deposit Account Number: ____ Deposit Account Name: ____

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☐ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☐ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	0.00
Design	200	100	100	50	130	65	0.00
Plant	200	100	300	150	160	80	0.00
Reissue	300	150	500	250	600	300	0.00
Provisional	200	100	0	0	0	0	0.00

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims ____ - 20 or HP = **Extra Claims** ____ x **Fee ($)** ____ = **Fee Paid ($)** 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims ____ - 3 or HP = **Extra Claims** ____ x **Fee ($)** ____ = **Fee Paid ($)** 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims
Fee ($) ____ **Fee Paid ($)** 0.00

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets ____ - 100 = **Extra Sheets** ____ / 50 = **Number of each additional 50 or fraction thereof** ____ (round **up** to a whole number) x **Fee ($)** ____ = **Fee Paid ($)** 0.00

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount) 0.00

Other: Appeal Brief 500.00

SUBMITTED BY			
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Name (Print/Type)	Susan M. Luna		Date April 28, 2005